A New Powerful Scalable Generic Multi-Standard LDPC Decoder Architecture

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Abstract

We propose a new powerful scalable generic parallel and modular architecture well suited to LDPC code decoding. This architecture template has been instantiated in the case of the 802.16e WiMax standard. The proposed design is fully compliant with all the code classes defined by the standard. It has been validated through an implementation on a Xilinx Virtex5 FPGA component. A four or six-module FPGA design yields a throughput ranging from 10 to 30 Mbit/s by means of 20 iterations at a clock frequency of 160 MHz which mostly satisfies communication throughput in the case of the WiMax Mobile communication.

1 Introduction

Low density parity-check (LDPC) are linear block codes. They have recently been included as error correcting codes in several new communication standards. A codeword of an (n, k) LDPC code must satisfy $m = n - k$ parity check equations on its n codeword bits. The whole set of $(n - k)$ equations can be depicted by means of a bipartite graph, composed of two kinds of nodes: *bit nodes* (*BN*), representing the bits of the codeword and *check nodes* (*CN*), representing the parity check equations. It can also be represented by a sparse parity check matrix H of size m-by-n, where n is the length of the code and m is the number of parity-check bits in the code, specifying the parity-check constraints of the bits in the codewords.

Even if the upcoming WiFi, WiMax and DVB-S2 standards adopt architecture-aware LDPC codes [5], the decoder realization is still a real challenge because of their huge data processing, and also their storage and network interconnection requirements. The hardware realization of an LDPC decoder is determined by many strongly interrelated parameters, leading to a large design space and various implementations [1, 4, 6, 2].

In this paper, we propose a new powerful scalable generic parallel and modular architecture well suited to LDPC code decoding. The size of the architecture in the case of a given standard and a given throughput is established during the space exploration process thanks to our optimization system based on a constraints programming approach.

2 Proposed Architecture

The architecture is illustrated in figure 1. It is made up of several processing modules communicating through an optimized interconnection structure. Each processing module includes two processing units (called bit node and check node), and a set of memory banks. The size of the architecture– number of modules, number of interconnection buses, size and number of memory banks– is both communication standard and throughput dependent.

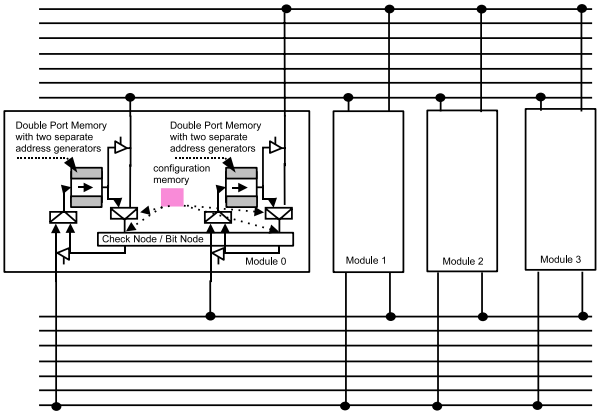

Figure 1. Organization of the parallel generic architecture.

Our approach consists in clustering nodes of the whole set of CN nodes (respectively BN nodes) into independent sets called CS (respectively BS) according to the features of the parity check matrix H. All nodes of a given CS or BS set are processed in the same computation unit called a *module*. All the nodes of the set are then processed sequentially. According to the degree of parallelism of the architecture (number of modules), nodes of different CS sets (respectively BS) can be processed in parallel on different *modules*. Each *module* has its own local memory used

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for storing the exchanged messages between check nodes and bit nodes during the computation process (corresponding to the edges of the bipartite graph). Each local memory is composed of several memory banks allowing parallel accesses to be performed. The basic idea is that all components of a message can be accessed simultaneously. Each module is able to process check nodes as well as bit nodes. In the case of check node processing, the data comes from their local memories. The local memories of the module contain all the messages coming from the related BS. After the processing accomplished in the module, results are stored in the same local memories. In the case of bit node processing, the data can come from local or non-local memories according to the corresponding parity matrix. In the case of non-local memory, a data transfer through the interconnection structure is performed.

3 Case Study

Table 1 summarizes the results of the architecture exploration phase which allows different configurations of the architecture to be compared. For each code ratio of the WiMax LDPC standard [3], the table gives, for a given number of modules, an optimal solution in terms of CN set quantity per module, bus quantity of the interconnection structure, scenario quantity required for the computation of the BN sets and memory size required to store the messages during the decoding.

Code	Modules	Sets per module	Buses	Scenarii	Memory size (6-bit word)
1/2	3	4	8	8	2592
	4	3	10	6	2880
	6	2	22	4	6336
2/3A	4	2	10	6	1920
2/3B	4	2	11	6	2112
3/4	3	2	15	8	2160
5/6	2	4	20	12	1920
	4	1	20	6	1920

Table 1. Optimal solutions for WiMAx ratios.

Table 1 shows that a parallel architecture composed of 4 modules connected to a 20-bus interconnection structure is able to support all the WiMax code. Each module is in charge of at most three CS sets. It includes a local memory organized into 20 banks of 3×96 words.

PM	FFs	Memory 18kb block	Slice LUT	Max Frequency MHz
4	10K (14%)	92	19K (27%)	192

Table 2. Implementation results of the IP on a Xilinx Virtex5 110LXT.

A synthesizable generic VHDL IP core, fully compliant with the 802.16e standard, has been developed. It covers all the modes and ratios defined in the standard. Our generic IP core allows to switch from one ratio to another on-the-fly. The core has been synthesized with Xilinx XST on a Virtex5 LX110T target. Table 2 gives the implementation results of the IP for a four processing module (PM) configuration.

Table 3 gives some results obtained in the case of different configurations: 1, 4 and 6 processing modules. The system performances are expressed by: the number of cycles required for the execution of one algorithm iteration and the throughput of the IP in Mbit/sec (output payload stream rate after redundancy suppression) for 20 iterations and a 160 MHz system clock.

PM		ratio 1/2	ratio 2/3A	ratio 2/3B	ratio 3/4A	ratio 3/4B	ratio 5/6
1	cycles/block	884	788	788	740	740	692
	Throughput	2.6	3.94	3.94	4.74	4.74	5.27
4	cycle/block	236	212	212	212	212	188
	Throughput	10.4	15.8	15.8	19.2	19.2	21.6
6	cycle/block	164	164	164	140	140	140
	Throughput	14.84	19.78	19.78	26.34	26.34	29.26

Table 3. Performance results of the LDPC decoder.

4 Summary

We have presented a new powerful scalable generic parallel and modular LDPC architecture. An IP core fully compliant with all the modes of the 802.16e WiMax standard has been developed and synthesized on a Xilinx Virtex5. A four or six-module FPGA design yields a throughput ranging from 10 to 30 Mbit/s at a clock frequency of 160 MHz. This frequency range is compatible with the throughput requirements of the WiMax mobile standard. Future work will consist in applying the principles of this scalable generic parallel architecture to other communication standards such as the 802.11n standard. It will also include further optimizations.

References

[1] A. Blanksby and C. Howland. A 690-mW 1-Gb/s 1024-b, Rate-1/2 Low-Density Parity-Check Code Decoder. *IEEE Journal of Solid-State Circuits*, 37(3):404–412, March 2002.

[2] M. Cocco, J. Dielissen, M. Heijligers, A. Hekstra, and J. Huisken. A Scalable Architecture for LDPC Decoding. In *Proceedings of DATE 2004*, pages 88–93, 2004.

[3] IEEE 802.16e. Air Interface for Fixed and Mobile Broadband Wireless Access Systems. IEEE P802.16e/D12 Draft, October 2005.

[4] F. Kienle, T. Brack, and N. Wehn. A Synthesizable IP Core for DVB-S2 LDPC Code Decoding. In *Proceedings of DATE 2005*, pages 100–105, 2005.

[5] M. Mansour and N. Shanbhag. High-Throughput LDPC Decoders. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 11(6):976–996, Dec. 2003.

[6] P. Urard, L. Paumier, P. Georgelin, T. Michel, V. Lebars, E. Yeo, and B. Gupta. A 135Mbps DVB-S2 Compliant Codec based on 64800-bit LDPC and BCH Codes. In *Proceedings of DAC 2005*, pages 547–548, June 2005.